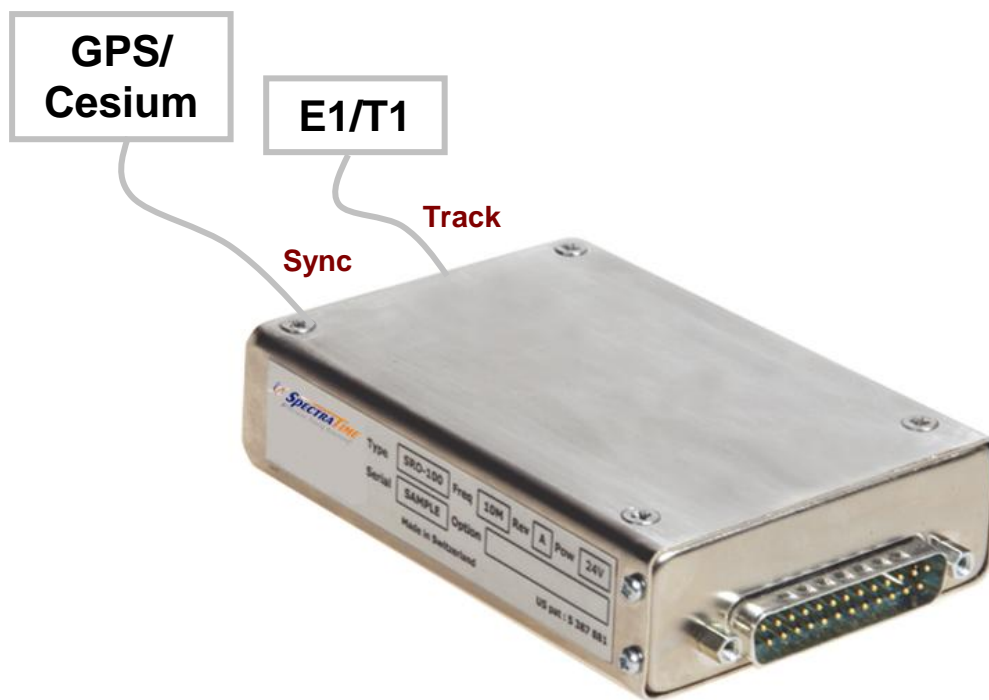


Low Cost GPS/E1/T1/Cesium-Synchronized Rubidium Oscillator (SRO-100)

Patented SRO-100 SynClock+[®]
Auto-Adaptive SmartTiming+[®] Disciplining & Filtering @ 1ns Resolution



APPLICATIONS

Telecom | Navigation | Broadcast | Defense | Instrument

KEY FEATURES

Smart SRO-100 SynClock+[®]

- Single power supply voltage : 11 - 16V or 20 - 32V
- Small volume : 11 in³ (2.78x4x1")
- Frequency offset over temp. range : ± 1E-10
- Short-term stability : 1E-12 / 100 sec.
- Industry's first SmarTiming+[®] technology
 - REF locking resolution : 1 ns
 - REF disciplining/filtering/controlling : Auto adaptive^(a)
 - Smart loop time constant : 1000 - 100,000 sec
 - E1/T1 jitter & wander : ITU-T G.823/824
 - REF locking mode (user settable) : Sync^(b) or Track^(c)
 - REF types (PRS^(d)/Stratum 1 source) : GPS, Cesium, E1/T1, LORAN-C, Maser
 - OUT frequency accuracy/stability
 - PRS^(d)/Stratum 1 locked : 1E-12, typical
 - Holdover (No PRS^(d)) : <5E-11/month
 - OUT time accuracy/stability
 - GPS locked : <50ns
 - Holdover (no GPS) : <2µs/48 hr or <1µs/24 hr
 - Standards compliance
 - PRS^(d) locked/unlocked : ANSI T1.101, Stratum 1 / 2, GR-1244
ITU-T G.811/G.812, PRC, Type II
CDMA IS-95, UMTS 3GPPS 25.104
- Low warm-up current : < 1.2A
- Ultra low aging : < 5E-11/ month
- Ultra low phase noise output : 10MHz -100dBc @ 10 Hz
- High frequency LV CMOS output : 60MHz
- RS232 standard interface : Control & monitoring commands, 9600 b/s

Notes

- (a) Request our **SmarTiming+[®] Technology White Paper** to compare performance at SynClock@spectratime.com
- (b) REF/OUT phase alignment
- (c) REF/OUT frequency alignment
- (d) PRS: Stratum 1 Primary Reference Source such as GPS, Cesium, E1/T1, LORAN-C, Maser

REVISION TRACKING LIST

Software Revision			Hardware Revision
Date	Version	Comment	
11 Jun 2002	1.01	Internal Correction	
09 Jul 2002	1.02	Now commands PW and TC store data in EEPROM	
23 Jul 2002	1.03	Internal Correction	
19 Sep 2002	1.04	New command "MCsdd" for interfacing with GPS receiver	
27 Sep 2002	1.05	Internal Correction	
07 Feb 2003	1.06	New command DT, Date. New command COsddd, time comparator offset	
11 Mar 2003			New low power version <17W
19 Aug 2003	1.07	Improved behavior at the start of tracking. Frequency save (FSx) improved. Command MCsdd extended. New commands VS, view PPSRef stability, VT, view time constant. Internal corrections	
23 Sep 2003	1.08	New command RAsddd. Internal corrections.	
25 Feb 2004	1.09	Back to simple start of tracking. GPS messages for Jupiter-Pico, SuperStar II. NMEA messages.	
05 Sep 2007	1.095	Other initial settings	

SPECIFICATIONS**ELECTRICAL**

Spec	Smart SRO-100 SynClock+®			
Type	Standard	Options		
RFOUT Frequency	10 MHz	Optional 5 MHz, 15 MHz (ordering code: 5M or 15M)		
Frequency Change Operating temperature range <i>(Thermal chamber with air flow)</i>	< 1E-10 -20°C to +60°C	-30 to 65°C (ordering code: E) -10 to 60°C (ordering code: LP)		
Frequency Accuracy @ Shipment	< 5E-11 (+25°C), typical			
Aging <i>(After 3 months of continuous operation)</i>	< 5E-11 / month (typical: 3E-11 / month)	< 3E-11 / month or 2E-10 / year (ordering code: A) (typical: ±1E-11 / month)		
Short Term Stability		(ordering code: S)		
	1s	3E-11	1E-11	
	10s	1E-11	3 E-12	
	100s	3E-12	1E-12	
Phase Noise (dBc/Hz) <i>(RFOUT 10 MHz)</i>			(ordering code: S)	
	1 Hz	-75	-80	
	10 Hz	-95	-100	
	100 Hz	-125		
	1k Hz	-145		
	10K Hz	-145		
Frequency Retrace Off/On <i>(In stable temperature, gravity, pressure & magnetic field conditions)</i>		< 5E-11 24 hr / 1 hr		
Warm-up Time @ +25°C Frequency stability	12 min 5E-10	7 min 5E-10 (ordering code: F)	< 4min 5E-10 (ordering code: FE)	25 min 5E-10 (Low Power ordering code: LP)
Analog Frequency Adjustment Tolerance <i>[An external voltage (0-5 VDC) can be applied to pin 6 (FA). The cursor pin of a 10 kΩ variable resistor placed between pin 7 and GND can provide this voltage. If not used, pin 7 must be floating]</i>	$5 \times 10^{-9} \pm 20\%$			
Digital Frequency Adjustment Internal crystal oscillator freq. Resolution <i>(Through RS-232 commands)</i>	±1.67E-8 60MHz 5.12E-13			
RFOUT Output level Output impedance Harmonics Spurious $f_0 \pm 100\text{kHz}$ 60MHz sub-harmonics	Sine wave 0.5 Vrms ($\pm 10\%$ / 50Ω) 50 Ω $\pm 20\%$ < -25dBc < -80dBc < -45dBc			

ELECTRICAL

Spec	Smart SRO-100 SynClock+ [®]		
60MHz Out	Square wave 3.3V LV CMOS		10 MHz Square wave 3.3V (ordering code: LVCMOS)
Supply Voltage (DC)	24V (20 to 32 V)		12V (11.2 to 16 V) (ordering code: 12V)
Max Power Supply Ripple	< 50 mV peak to peak (from 1Hz to 1 MHz frequency band)		
Input Power	With following options		
Warm up @+25°C (typical)	<28W @12V or <35W @ 24V	(F/E)	(FE)
0°C		<40 W	<50 W
+25°C		<14 W	<17W
+60°C		< 11 W	
Communication Interface	RS-232 commands for control & monitoring (see commands below) Timing and locking control functions VMGA messages		
Protocol speed	9600, n, 8, 1		
Compatible with	SRO model		
Conformal coating	None	Yes (ordering code: CC)	
Reverse Voltage Protection	< -40V (up to -40V on power input / no damage)		

SMARTIMING+[®] DISCIPLINING & FILTERING

Spec	Smart SRO-100 SynClock+ [®]		
PPSREF Level	CMOS 0-5V or 0-3.3V rising edge		
Reference types	GPS, E1, T1, Cesium, LORAN-C, Maser, etc		
Disciplining & filtering	Auto-adaptive through SmartTiming+ [®] technology (request white paper)		
Disciplining mode	Sync (phase alignment) or Track (frequency alignment)		
Architecture Model	See Principles of Operation below		
GPS Receiver Control	(Request GPS/SRO Connectivity AppNote)		
T-RAIM	Auto-configured at startup, if supported by GPS		
Position hold	Auto-configured at startup, if supported by GPS		
PPSOUT Output Level	CMOS 0-5V		
Current	+20 mA sink/source		
PPSOUT Adjustable Duty Cycle	133 ns step from 0 to 1sec		
Pulse Width (PW)			
PPSOUT to PPSREF Sync Error	< 50 ns		
Conditions (Sync Mode)	No PPSRef noise, ± 1°C temp fluctuations		
PPSOUT to PPSREF (DE)	0 to 1s in 133ns/step		
Programmable delay (Track mode)			
PPSOUT Holdover Time Stability	< 1µs / 24 hr	< 3µs / 24 hr	< 7µs / 24 hr
Temperature window	< 7µs / 1 week	Within 20°C	Within 40°C
(After learning phase > 10 τ)	Within ±2°C		
Smart Loop Time Constant	Auto-adaptive 1,000 to 100,000 sec		
Phase/Frequency	Sync/Trak mode		
User settable	RS-232 command interface		

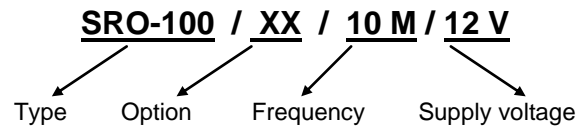
ENVIRONMENTAL

Spec	Smart SRO-100 SynClock+ [®]		
Magnetic Field Sensitivity	< 2E-10 / Gauss in worst axis		
Storage Temperature	- 55°C to + 85°C		
Humidity	GR-CORE-63, Section 5.1.2		
Operating Vibration	GR-CORE-63, Section 5.4.2		
Shock	Random and Sinusoidal MIL-PRF-28800F, Class 3, 4		
Survival	40g / 11ms		
Helium concentration sensitivity	< 1E-10 per ppm of Helium concentration change		
G-Tip-Over Test	< 2E-10 / g in worst axis		
Shielding	Soldered packaging (ordering code: SH)		

PHYSICAL

Spec	Smart SRO-100 SynClock+®
Size (L x W x H)	4" x 2.78 " x 1" (101.6 x 70.61 x 25.4 mm)
Weight	234g (8.25oz)
Mounting & Mechanical Layout	See drawings below
Connector	Male D-sub 25 pins (see drawing below)
Compatible with	SRO model

MODEL ORDERING INSTRUCTIONS



KEY PRINCIPLES OF OPERATION

SmarTiming+[®] SRO SynClock+[®]

The smart SRO SynClock+[®] uses SmarTiming+[®] technology. It auto-adaptively locks multi-vendor Stratum-1 references such as GPS, Cesium, LORAN-C, CDMA and E1/T1 at industry’s first 1ns resolution for the highest performance level, and generates a perfectly aligned 1PPS output signal (PPSOUT) and time of day (TOD) information.

As illustrated in Fig. 1 below, the smart SRO has two basic modes of operation: “Track” and “Sync”. “Track” is used for frequency alignment while “Sync” is used for phase alignment applications.

In “Track” mode, the smart SRO uses an external PPS reference (PPSREF) to align the frequency of the SRO. The frequency alignment is computed by an internal phase-time error signal that is generated by an internal PPS signal (PPSINT), which measures the signal at 1 ns resolution through its SmarTiming+[®] technology. The PPSINT then aligns the PPSREF phase.

In the “Sync” mode, the smart SRO phase aligns the PPSOUT to the PPSREF with the PPSINT reference signal, which uses SmarTiming+[®] algorithm to 1) compare the PPSOUT and PPSREF signals at 1ns resolution within a +/-500ns dynamic range and 2) auto-adaptively align them.

The smart SRO has also the capability to dynamically analyze the stability of the PPSREF signal through the excellent mid-term frequency stability of the Rubidium technology. Thus, the 1PPS reference of a Stratum-1 source such as GPS can be directly fed to smart SRO without specific analysis of the internal optimization parameters of the GPS engine - i.e., number of satellites in view, signal to noise ratio, etc.

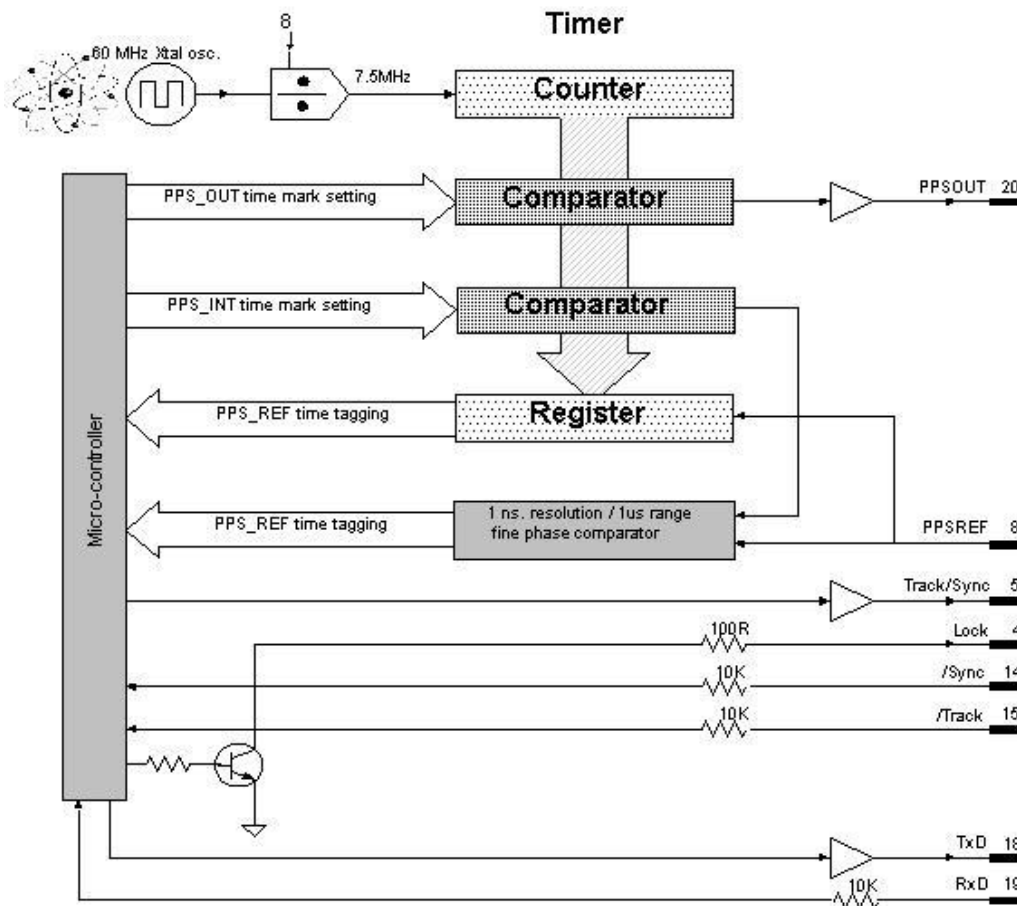


Fig.1: SmarTiming+[®] Control Block Diagram

As illustrated in Fig. 2 below, the “Track” mode aligns the PPSINT to the PPSREF within 133ns. After about 10τ, the PPSINT is perfectly aligned to the PPSREF.

The smart SRO is also capable to perfectly align the PPSOUT to the PPSREF or to adjust the PPSOUT from 0-1s with a 133ns resolution. This time adjustment can be programmed through the RS232 interface. After a descending edge of the "Sync" signal, the PPSOUT will be aligned to the PPSREF (see figure 2).

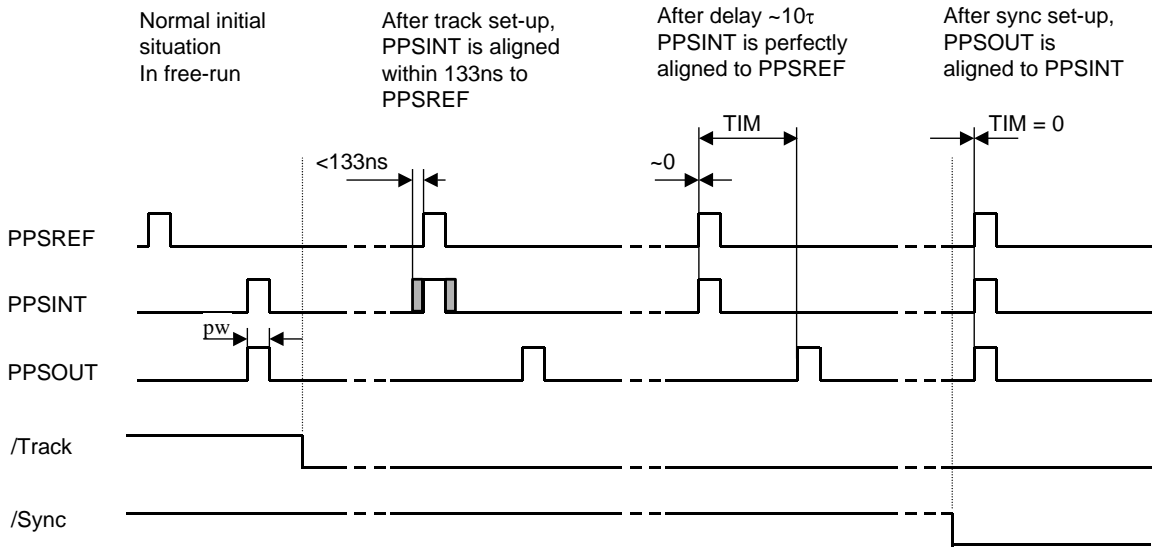


Figure 2 : "Track" & "Sync" Mode

STANDARD RS-232 CONTROL & MONITORING COMMANDS

Frequency Adjustment & Monitoring Functions

The operating and monitoring parameters of the SRO SynClock+[®] are accessible for read and write operations through the serial RS-232 port (9600 bits/sec., no parity, 1 start bit, 8 data bits, 1 stop bit).

There are 2 basic commands, which are *M, Cxxxx*

M<CR><LF>: monitors the basic internal signals of the atomic clock.
The returned answer looks like

HH GG FF EE DD CC BB AA <CR> <LF>

Where each returned byte is an ASCII coded hexadecimal value, separated by a <Space> character. All parameters are coded at full scale.

- HH*: Read-back of the user provided frequency adjustment voltage on pin 2 (0 to 5V)
- GG*: reserved
- FF*: peak voltage of Rb-signal (0 to 5V)
- EE*: DC-Voltage of the photocell (5V to 0V)
- DD*: varactor control voltage (0 to 5V)
- CC*: Rb-lamp heating current (Imax to 0)
- BB*: Rb-cell heating current (Imax to 0)
- AA*: reserved

*Cxxxx<CR><LF> **: output frequency adjustment through the synthesizer, by steps of 5.12×10^{-13} , where *xxxx* is a signed 16 bits word in hexa coded ASCII. This value is automatically stored in a EEPROM as last frequency which is applied after RESET or power-ON operation.
In Track mode this correction is not in use. The function *FCsdddd* do the same. But the data format is different.

* Warning :: This command is acting into non volatile memory. Numbers of commands sent during the whole unit life time limited to 10'000 in total (all commands cumulated).

Timing & Locking Control Functions

Using the same data interface, the smart SRO SynClock+® models can accept the following basic ASCII commands: Data is in decimal ASCII code.

Command name	Syntax command	Data field (if any)	Response syntax	Response data (if any)
Identification	ID<CR><LF>	-	TNTSRO-aaa/rr/s.ss <CR><LF>	aaa: 100 rr: revision number s.ss: software version
Serial number	SN<CR><LF>	-	xxxxxx<CR><LF>	xxxxxx : 6 digits serial nbr
Status	ST<CR><LF>	-	s<CR><LF>	s:Status s=0 :warming up s=1 :tracking set-up s=2 :track to PPSREF s=3 :synch to PPSREF s=4 :Free Run. Track OFF s=5 :FR. PPSREF unstable s=6 :FR. No PPSREF s=7 :factory used s=8 :factory used s=9 :fault or Rb OOL
Set Tracking PPSINT - PSSREF	TRx<CR><LF> *	x=0 : Track never * x=1 : Track now x=2 : Track ever * x=3 : Track now + ever * x=9 : Interrogation	x<CR><LF>	x:Tracking commands status x=0 : Track OFF x=1 : Track ON (when Status 9 -> 4
Set Synchronisation PPSOUT – PPSINT	SYx<CR><LF> *	X=0 : Synch. never * x=1 : Synch. now x=2 : Synch. ever * x=3 : Synch. now + ever * x=9 : Interrogation	x<CR><LF>	x:Synch. commands status x=0 : Synch. OFF x=1 : Synch. ON (When Status 1 -> 2)
Set PPSOUT delay	DEdddddd<CR><LF>	dddddd=delay by 133ns step. Max 7499999 DE0000000 :synch to PPSREF	dddddd<CR><LF>	dddddd=delay by 133ns step. Max 7499999
Set PPSOUT Pulse Width	PWdddddd<CR><LF> *	dddddd=pulse Width by 133ns step. Max 7499999 PW0000000: no pulse	dddddd<CR><LF>	dddddd=Pulse Width by 133ns step. Max 7499999 0000000: no pulse
Time of day	TD<CR><LF>	-	hh:mm:ss<CR><LF>	hh:hours mm:minutes ss:seconds
Set time of day	TDhh:mm:ss<CR><LF>	hh:Hours mm:Minutes ss:seconds	hh:mm:ss<CR><LF>	hh:hours mm:minutes ss:seconds
Date	DT <CR><LF>	-	yyyy-mm-dd	yyyy : year mm : month dd : day
Set date	DT yyyy-mm-dd <CR><LF>	yyyy : year mm : month dd : day	yyyy-mm-dd	yyyy : year mm : month dd : day
Beat every second on serial port.	BTx<CR><LF>	x=0 : Stop beat x=1 : Effective Time interval PPSOUT vs PPSREF x=2 : Phase comparator x=3 : Both x=1 & x=2 x=4 : Beat Time of day x=5 : Beat status x=6 : Beat <CR><LF> x=7 : Beat Date, Time, Status x=A : Beat NMEA \$PTNTA, x=B : Beat NMEA \$PTNTS,B,	dddddd<CR><LF> or sppp<CR><LF> or dddddd sppp <CR><LF> or hh:mm:ss<CR><LF> s<CR><LF> <CR><LF> yyyy-mm-dd hh:mm:ss s	dddddd : delay in 133ns step sppp:phase error in ns s: +/- signe hh:hours mm:minutes ss:secondes s: status yyyy:year, mm:month,dd:day
Set frequency adjustment	FCsdddd<CR><LF> *	s=+/- signe dddd = limited within range : +32767/-32768 FC+99999 : interrogation	sdddd<CR><LF>	s: +/- signe dddd : frequ. Adj. in 5.12 x 10 ⁻¹³ step

Command name	Syntax command	Data field (if any)	Response syntax	Response data (if any)
Set frequency save. Integral part, when Status = 2, 3	FS <CR><LF> *	x=0 : never save x=1 : save every 24 hours x=2 : save right now x=3 : save actual freq. now x=9 : interrogation	x<CR><LF>	x=0 : never save x=1 : save every 24 hours
Set Tracking Window	TW ddd<CR><LF> *	ddd = Half Tracking Window by 133ns step. From 1 to 255 ddd = 999 : interrogation	ddd<CR><LF>	ddd : Half Tracking Window by 133ns step.
Set no Alarm Window	AW ddd<CR><LF> *	ddd = Half no Alarm Window by 133ns step. From 1 to 255 ddd = 999 : interrogation	ddd<CR><LF>	ddd : Half no Alarm Window by 133ns step.
Set tracking phase loop time constant	TC dddddd<CR><LF> *	dddddd = Time constant in seconds (001000 to 999999) TC000000 : change to auto. (<)TC001000 : no change	Dddddd<CR><LF>	dddddd : time constant in seconds
Set module customization	MC sxx [cc...c] <CR><LF> *	s = L : Load parameter s = S : Store parameter ccc..c * s = B : Load start behaviour s = A : Activate msg at start * s = C : Cancel msg at start * s = H : Load Help s = T : Load Data Type xx = 00..FF: msg number, ccc...c : new welcome message, up to 24 characters	cc..c<CR><LF> or d<CR><LF> or xy<CR><LF>	ccc..c : response to MCLxx or to MCHxx. d : 0, 1 response to MCBdd or xy : Data Type, response to MCTxx, x=0 RAM, x=1 eeprom, x=2 Flash, y=0 Byte, y=1 sByte, y=2 Word, y=3 sWoord, ... y=8 string ASCII, y=9 strng binary
Set phase comparator Offset	CO sddd<CR><LF> *	s : +/- signe ddd : limited with range + 127 / - 128 CO+999 : interrogation	sddd<CR><LF>	s : +/- signe ddd : offset in approx 1 ns steps
View PPSRef Sigma	VS <CR><LF>		ddd.d<CR><LF>	ddd.d : Sigma of PPSRef in ns. In tracking, Status 2, 3.
View Time constant	VT <CR><LF>		dddddd<CR><LF>	dddddd : Loop time constant now in use, in ns.
Raw phase adjust	RA sddd<CR><LF>	s : +/- signe ddd : limited with range + 127 / - 128	sddd <CR><LF>	s : +/- signe ddd : raw phase just asked in 133 ns steps
Reset micro controller	RESET <CR><LF>			(Identification & welcome message, GPS binary)

*Warning : These commands are acting into non volatile memory. Numbers of commands sent during the whole unit life time limited to 10'000 in total (all commands cumulated)
But TR1 followed by TR0 and SY1 followed by SY0 don't write in NVM

PIN # 4 & 5 STATUS LEVELS			
Status	Pin # 4	Pin # 5	
	Xtal not locked to Rb line Rb lock (open collector)	In Track Mode (TTL + 1K)	In Synch Mode (TTL + 1K)
s=0 :warming up	Low (<.2 V / 5 mA)	High	High
s=1 :tracking set-up	High	High	High
s=2 :track to PPSREF	High	Low	High
s=3 :synch to PPSREF	High	High	Low
s=4 :Free Run. Track OFF	High	High	High
s=5 :FR. PPSREF unstable	High	High	High
s=6 :FR. No PPSREF	High	High	High
s=7 :factory used	High	High	High
s=8 :factory used	High	High	High
s=9 :fault or Rb OOL	Low (<.2 V / 5 mA)	High	High

NMEA 0183 Format (BTA, BTB)

\$PTNTA,yyyymmddhhnnss,q,T3,rrrrrr,sfff,x,y*CS<CR><LF>

yyyy: year; mm:month; dd: day; hh: hour; nn: minute; ss: second; q: quality, 0: Rb line not locked, 1: Free Run, 2: Disciplined; T3: format descriptor; rrrrrr: effective time interval PPSOUT vs PPSREF; sff: phase comparator; x,y: reserved; CS: checksum.

\$PTNTS,B,s,ffff,iiii,aaaa,x,y,s,ccccc,ggg.gg,x,y*CS<CR><LF>

s: general SRO status; ffff: actual frequency offset; iiii: integral part of PI regulator; aaaa: average frequency on 24 hours; x,y: reserved; ccccc: loop time constant; ggg.gg: sigma; x,y: reserved; CS: checksum.

PIN-OUT DESCRIPTION

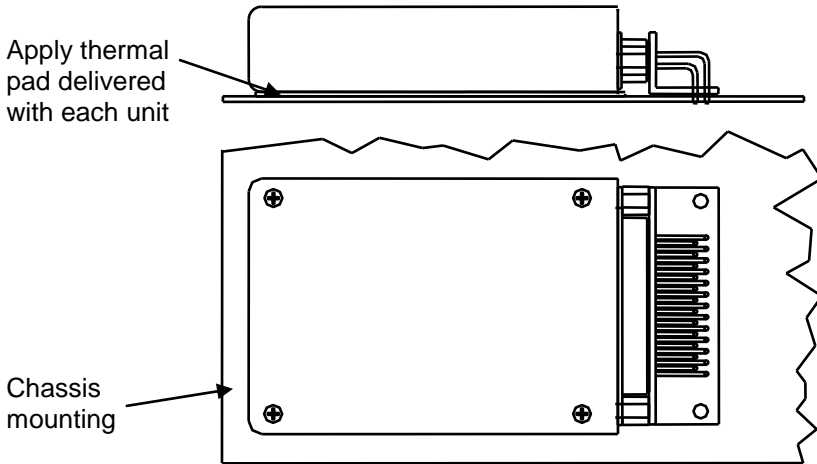
Pin #	Smart SRO-100 SynClock+ [®]	Dir
1	12V(11.2 to 16) or 24V (20 to 32)	Input
2	12V(11.2 to 16) or 24V (20 to 32)	Input
3	GND	Ret
4	Rb lock (open collector) (lock=open)	Output
5	Track/Synch Alarm (TTL+1K) (lock=0V)	Output
6	FA (analog frequency adjust input)	Input
7	Vref out (+5V internal reference)	Output
8	PPSREF (reference time pulse)	Input
9	NC (Factory use or diagnostics)	Output
10	GND	Ret
11	Factory Use	NA
12	GND	Ret
13	60M (60 MHz square 3.3V output) or (10 Mhz Square wave 3.3V option LVCMOS)	Output
14	/Sync (synchronize PPSOUT to PPSREF)	Input
15	/Track (PPSREF phase tracking)	Input
16	NC (Factory use or diagnostics)	In-Out
17	/Reset (SRO micro controller)	Input
18	TxD (RS232 Transmit 0-5V)	Output
19	RxD (RS232 Receive 0-5V)	Input
20	PPSOUT (output time pulse from internal clock)	Output
21	GND	Ret
22	GND	Ret
23	GND	Ret
24	RFOUT (5 or 10 or 15MHz sinus 7dBm into 50Ω)	Output
25	GND	Ret

MOUNTING & MECHANICAL LAYOUT

Mounting Layout

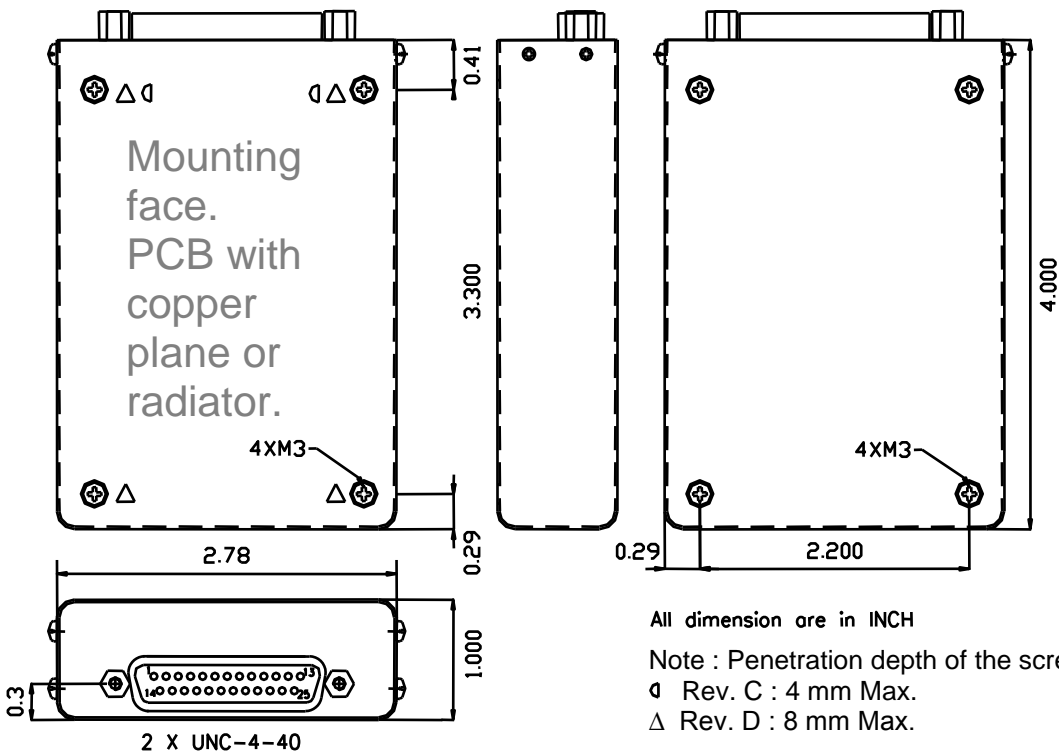
Heat sink options:

- 1) Mount the SRO on a copper ground PCB with the provided thermal pad or thermal paste in between and a base plate under the PCB
- 2) Mount the SRO against a system chassis using the 4xM3 screws with the provided thermal pad or thermal paste in between and wire bridge the D-Sub connector
- 3) Mount a radiator on top of the SRO with the provided thermal pad or thermal paste in between, if no base plate is available

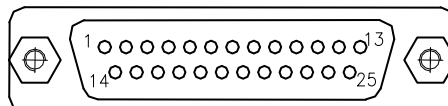


Mechanical Layout & Dimensions (SRO-100)

All dimensions in inch (") and the pictures are not to scale.



Connector Front View (SRO-100)



Male D-Sub 25 pins